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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,012	11/24/2003	Seong-Ho Jeung	8836-198 (IB12226-US)	5661
22150	7590	04/04/2005	EXAMINER	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,012	JEUNG, SEONG-HO	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-4,6-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuda et al. (U.S. Patent No. 6,646,900).

Regarding claims 1, 9, 15, Tsuda et al. disclose a ternary content addressable memory ("CAM") cell (Figure 1) comprising:

- a main memory cell (12) enabled to a wordline (WL) to store data;
- a mask memory cell (14) enabled to the wordline to store mask data;
- a bitline pair (DBIT, DBITN) for transmitting the data to or from the main memory cell ;
- a mask bitline pair (MBIT, MBITN) for transmitting the mask data to the mask memory cell;
- a comparison signal line pair (Figure 2A, CMPN, CMP) for transmitting comparison data;
- a match line (ML);
- a mask circuit (Figure 2A, 18) for receiving the mask data, the mask circuit being coupled to the match line and the mask memory cell (Figure 2A, 18 coupled to ML and mask cell by MN) ; and
- a comparison circuit (Figure 2A, 20, 22,24, 26) including a pair of transistors coupled to the comparison signal line pair (22, 26, coupled to comparison pair CMPN, CMP) and a pair of match transistors (20,24, coupled to data lines D, DN) coupled to data of the main memory cell , the comparison circuit being coupled to a ground line of the mask circuit (Figure 2A comparison circuit 20,24,22,26 coupled ground line of mask circuit 18).

Regarding claims 2-4, 5-14, 16-20, Tsuda et al. disclose characterized in that the comparison circuit includes a first NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the comparison data; a second NMOS transistor having a drain coupled to the mask circuit and a gate coupled to a comparison data line; a first match NMOS transistor having a drain coupled to the first NMOS transistor, a gate coupled to the data of the main memory cell, and a source coupled to a ground voltage, and a second match NMOS transistor having a drain coupled to the second NMOS transistor, a gate coupled to complementary data of the main memory cell, and a source coupled to a ground voltage (Figure 2A of Tsuda clearly disclosed a comparison as present invention discloses), and Tsuda et al. disclose characterized in that the comparison circuit includes a first match NMOS transistor having a drain coupled to the mask of the main memory cell; a second match NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the data circuit and a gate coupled to the complementary data of the main memory cell; a first NMOS transistor having a drain coupled to a source of the first NMOS transistor, a gate coupled to the comparison signal line, and a source coupled to a ground voltage, and a second NMOS transistor having a drain coupled to a source of the second NMOS transistor, a gate coupled to the comparison signal line, and a source coupled to a ground voltage, and characterized in that the mask circuit is an NMOS transistor which is coupled between the match line and the comparison circuit and is gated by the mask data (Figures 1-2A disclosed a comparison circuit and arrangement as claims 3-4 disclose).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda et al. in view of Gharia (U.S. Patent No. 6,760,241).

Tsuda et al. as described above in 102 rejection, fail to disclose a comparison circuit being coupled between the match line and the mask circuit. However, Figure 1 of Gharia disclose a comparison circuit 104 is coupled between a match line and a mask circuit 106. Since the comparison circuit 104 of Gharia has one end coupled to match line and another is coupled to masking circuit 106. Therefore, the comparison circuit is arranged between match line and mask circuit as claim 5 discloses.

As discussed above, it would have been obvious to one of ordinary skill in the art to arrange the position of comparison circuit between match line and mask circuit. Applicant has not disclosed that positioning of comparison circuit provides an advantage is used for particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the comparison circuit arranged to a ground line of the mask circuit as in claim 1 of present application because the comparison circuit in claim 5 of present invention ability to perform its function on receiving and transferring data is not effected by its location in memory device.

Therefore, it would have been obvious to a person of ordinary skill in this art to modify Gharia to obtain the invention as specified in claim 5.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2827